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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,063	03/01/2002	Dong-Seok Nam	8021-89 (SS-16177-US)	3231

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EXAMINER	
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ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,063	NAM ET AL.	
	Examin r	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication app ars on th cover sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11-14,22 and 23* is/are rejected.

7)☒ Claim(s) *4-9 and 15-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. The objection to claims 4 and 11 is withdrawn.

2. Claims 1-9 and 11-23 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 11-14, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US 6,352,896) in view of Chi (US 6,174,767) and Hurley (US 2003/0013253).

In re claim 1, Liu et al., in Figs. 2A, 4I and related text, teach the claimed semiconductor device, comprising:

- a semiconductor substrate 200 (Fig. 4I);
- an isolation layer 202 formed on the semiconductor substrate 200 for defining a plurality of active regions 204 (Fig.2A and 4I), each of the plurality of active regions 204 having a major axis (X axis) and a minor axis (Y axis);
- a plurality of gates 206/210 and 208/210 formed to cross the plurality of active regions 204 (Fig.4I) and extend in a direction of the minor axis of each of the plurality of active regions 204, each of the plurality of gates 206/210 and 208/210 having a first side (left side) and a second side (right side) that are opposing and that run along the direction of the minor axis;

- a plurality of first and second source/drain regions (not shown but stated in col. 3, lines 49-51) formed in the plurality of active regions 204 at either of the first side or the second side of each of the plurality of gates 206/210 and 208/210, each of the plurality of first and second source/drain regions having a top surface; and
- a plurality of first self-aligned contact pads (SACs) 222a and a plurality of second SACs 222b formed to contact the top surface of each of the plurality of first and second source/drain regions, respectively, wherein the plurality of first SACS pads 222a and the plurality of second SACs 222b are substantially the same size because 222a and 222b are formed with same width (Figs. 4I and 2D).

In contrast, Liu et al. do not teach that the plurality of first SACS pads 222a and the plurality of second SACs 222b are substantially the same top surface area.

Chi, in an analogous art, teach the plurality of first SACS pads and the plurality of second SACs PL1 are substantially the same top surface area (Fig.4B) because the plurality of SACs PL1 are formed via a same line-shape photoresist pattern AA (Fig.4A).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to modify the method of Liu et al. with the teachings of Chi so that the plurality of first SACS pads 222a and the plurality of second SACs 222b have the same top surface area, since by this modification it would simplify the entire structure, which is beneficial to a mass production of the device.

In re claim 2, Liu et al also teach that the plurality of gates 206/210 and 208/210 are formed such that each two of the plurality of gates 206/210 crosses one of the plurality of active regions 204 (Fig.2A).

In re claim 3, Liu et al. also teach that the isolation layer 202 has a top surface, and said semiconductor device further comprises a plurality of third SACs 222b formed to contact areas of the top surface of the isolation layer 202 that are disposed between adjacent first SACs 222a in a direction of the major axis of each of the plurality of active regions 204 (Fig.4I).

In re claim 11, Liu et al. also teach the claimed method for manufacturing a semiconductor device (Figs. 2A-2C, 4A-4I and related text), comprising the steps of:

- forming an isolation layer 202 on a semiconductor substrate 200, the isolation layer 202 for defining a plurality of active regions 204, each of the plurality of active regions 204 having a major axis (X axis) and a minor axis (Y axis);
- forming a plurality of gates 206/210 and 208/210 on areas of the semiconductor substrate 200 on which the isolation layer 202 is formed, the plurality of gates 206/210 and 208/210 formed to cross the plurality of active regions 204 (Fig.2A) and extend in a direction of the minor axis (Y axis) of each of the plurality of active regions 204, each of the plurality of gates 206/210 and 208/210 having a top surface and having a first side and a second side that are opposing and that that run along the direction of the minor axis;
- forming a plurality of first and second drain/source regions) (not shown) in the plurality active regions 204 at either of the first side or the second side of each of the plurality of gates 206/210 (col. 3,lines 49-51), each of the plurality of first and second source/drain regions having a top surface;
- forming a first interlayer insulating layer 216 on regions of the semiconductor substrate 200 on which the plurality of first and second source/drain regions are

formed, the first interlayer insulating layer 216 formed to completely fill spaces among the plurality of gates 206/210 and 208/210 and to have a planarized top surface(Fig.4B);

- forming photoresist patterns 218 in a line shape at each of a plurality of rows where an absence exists of any formation of the plurality of active regions 204 on the first interlayer insulating layer 216 (Fig. 2C);
- etching the first interlayer insulating layer 216 using the photoresist patterns 218 as etching masks to form a plurality of contact holes 220a through which the top surface of each of the plurality of first and second source/drain regions are respectively exposed (Fig.3C);
- removing the photoresist patterns 218 (Fig.3D); and
- forming a plurality of first self-aligned contact pads (SACs) 222a and a plurality of second SACs 222b to respectively contact the top surface of each of the plurality of first and second source/drain regions and to be level with the top surface of each of the plurality of gates 206/210 and 208/210, by filling the plurality of contact holes with a conductive material (Fig.4D).

In contrast, Liu et al. do not teach forming photoresist patterns in a line shape.

Chi, however, teaches using a line-shape pattern photoresist AA (i.e. SAC mask, Fig.4A) in forming SACs.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to modify the method of Liu et al. with the teachings of Chi so that the

photoresist pattern is in the line-shape, since by this manner it would simplify the manufacturing process.

In re claim 12, Liu et al. also teach that the plurality of gates 206/210 and 208/210 are formed such that each two of the plurality of gates 206/210 crosses one of the plurality of active regions 204 (Fig. 2A).

In re claim 13, Liu et al. also teach said step of forming the plurality of gates 206/210 and 208/210 comprises the steps of:

- sequentially forming a gate insulating layer (i.e. gate oxide, col.3, lines 34-36), a gate electrode 206 and 208, and a capping layer 210 on the areas of the semiconductor substrate 200 on which the isolation layer 202 is formed (Fig.4I);
- patterning the gate insulating layer, the gate electrode 206 and 208, and the capping layer 210 to form a patterned gate insulating layer, a patterned gate electrode, and a patterned capping layer; and
- forming gate spacers 212 to surround sidewalls of the patterned gate insulating layer, the patterned gate electrode, and the patterned capping layer, wherein the capping layer 210 and the gate spacers 212 are formed of an insulating material (silicon nitride) having a different etching selectivity from that of the first interlayer insulating layer (i.e. oxide) (col.4, lines 11-15).

In re claims 22 and 23, Liu et al. also teach that each of the photoresist patterns 218 are formed to include a protrusion as shown in Fig. 2C covering the first interlayer insulating layer 216 (Fig.4C), which is at the top surface of the isolation layer 202 positioned each of a plurality of rows whereat the plurality of active regions 204 are formed (Figs. 2C and 4C); and the

protrusion is formed to extend over any of the plurality of gates 206/210 and 208/210 that positioned at either a first opposing side or a second opposing side of the isolation layer 202, the first opposing side and the second opposing side of the isolation layer 202 being adjacent to at least one of the first side or the second side of at least one of the plurality of the gates 206/210 and 208/210.

Liu et al. in view of Chi teach the claimed limitations, as stated above, with the exception of forming a material layer that partially fills the spaces among the plurality of gates, subsequent to said step of forming the plurality of first and second source/drain regions, wherein the material layer is formed of an insulating layer having a different etching selectivity from that of the first interlayer insulating layer and is etched along with the first interlayer insulating layer.

Hurley, in an analogous art, teach forming a material layer 81 that partially fills the spaces among the plurality of gates 22/33/34/35/36 (Fig.8), subsequent to said step of forming the plurality of first and second source/drain regions 41 and 51, wherein the material layer 81 is formed of an insulating layer (i.e. titanium nitride barrier) having a different etching selectivity from that of the first interlayer insulating layer 64 (BPSG) and is etched along with the first interlayer insulating layer 64 (Figs. 7-8).

Therefore, one of the ordinary skilled in the art, at the time the invention was made, would have been motivated to forming a material layer partially filling the spaces among the gate, as taught by Hurley, in the method of Liu et al. in view of Chi, since by doing so it would prevent the gates from over-etching.

Allowable Subject Matter

5. Claims 4-9 and 15-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Liu et al. neither teach nor suggest forming a plurality of contact plugs through the first and the second interlayer insulating layers to respectively *contact the sidewalls and a predetermined portion of the top surface of each of the plurality of second SACs*; and forming a plurality of bit lines, each of the plurality of bit lines respectively formed along one of the plurality of second rows and extending in a direction of the major axis of each of the plurality of active regions, *the plurality of second rows corresponding to areas having an absence of contact between any of the plurality of active regions and a top surface of any of the plurality of contact plugs.*

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Examiner
Art Unit 2823

April 16, 2004